Sheet 6
MOS Logic Gates

Problem 1)

For the inverters below, find:
V_{OH} , V_{OL} , V_{IH} and V_{IL} In terms of transistors parameters.
Hint: Take $V_{Tn} = |V_{Tp}|$

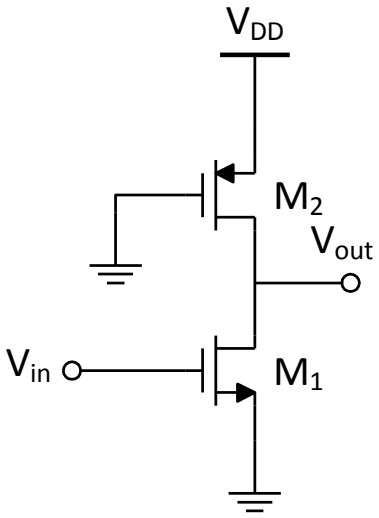

Figure (1)

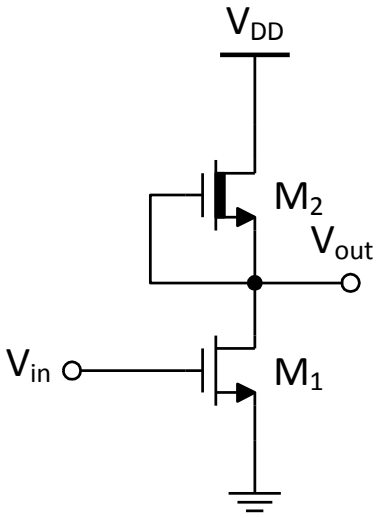

Figure (2)

Problem 2)

a) Implement the logic function (F' = ABC + DE') using static CMOS. Assume inverted inputs are available.

b) Size the transistors so that ($t_{pLH} = t_{pHL}$) in the worst case, and both are half the unit inverter delay.

c) Find approximate area of the gate designed if the technology used is 90nm.

d) Find the best case t_{pLH} and t_{pHL}.

Problem 3)

If C_L = 1 pF, and each internal node has 0.1 pF capacitor. Over two cycles:

a) What is the logic function of this gate?

b) What is the input pattern that causes worst charge sharing?

c) Find the value of the output voltage in this case.